REMARKS

Claims 1, 3-4, 6-12 and 16-21 are all the claims pending in the present application and stand rejected. Reconsideration and allowance of all pending claims are respectfully requested in view of the following remarks.

CLAIM REJECTIONS.

35 U.S.C. § 102

Claims 10, 12, 16 and 20-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,636,361 to Ingerman. Applicant respectfully traverses these rejections for the following reasons.

The Office Action alleges that Ingerman discloses all the features recited in these claims. As mentioned in the previous response, Ingerman discloses a multi-processor system having dual memory subsystems. That is, two processors 32, 50 and two bus/memory subsystem groups arranged so that each processor 32, 50 is connected with each bus to access separate memory subsystems via the associated bus. (Col. 6, ll. 27-34). The Office Action alleges that separate caches 34, 52 are analogous to Applicant's claimed memory array having first and second portions by interpreting "memory array" to include multiple separate devices. (5/25/04 Office Action page 7). However, the Office Action fails to provide any reasoning or evidence supporting this interpretation. The Examiner is respectfully reminded that during patent examination, the pending claims must be given the broadest reasonable interpretation which is consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). Applicant directs the Examiner to the embodiments disclosed at pg. 4, ll. 23 – pg. 5, ll. 18 and Figs. 1-3 of the application for guidance on the interpretation of "memory array" that is consistent with the specification.

Notwithstanding, Applicant amends claims 10 (and claims 12, 16 and 20-21 by virtue of their dependence on claim 10) to recite "a memory device" including a memory array with first and second portions. In view of the fact Ingerman fails to teach or suggest a memory device including a memory array whatsoever, reconsideration and withdrawal of this rejection is respectfully requested.

35 U.S.C. § 103

Claims 1, 3-4, 6-9 and 18-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,140,681 to Uchiyama in view of U.S. published application 2002/0184445 to Cherabuddi and/or Ingerman in view of Cherabuddi. Applicant respectfully traverses these rejections for the following reasons.

First, Applicant submits that there is no motivation in the references themselves for combining the references as suggested in the Office Action. Moreover, the Examiner's stated reason for modifying Uchiyama with Cherabuddi, i.e., to provide improved performance and efficient memory usage, is not a proper "objective" reason to combine references since it is purely speculation on behalf of the Examiner to suggest that dynamic adaptation of the size of copy-back regions 61 and 62 of main memory 5 of Uchiyama would even be desirable or provide any benefit whatsoever. Particularly, when the cited portions of Cherabuddi disclose dynamic allocation of cache resources ([0011]; Fig. 2) and the cited portions of Uchiyama addresses subdividing a main memory 5 (see Figs. 2 and 5). At most, the combination of Cherabuddi with Uchiyama, would teach the skilled artisan to dynamically adapt caches 3 and 4 (Fig. 2) of Uchiyama, as opposed to dynamically subdividing main memory 5.

As to the properness of combining Ingerman with Cherabuddi, the Office Action relies of various different memory devices (separate caches 34, 52 and main memories 42, 48) of Ingerman as a memory array, but somehow infers that the sizes of these distinctly different memory devices could be allocated based on the dynamic allocation of cache resources methods disclosed by Cherabuddi. Applicant is unable to comprehend the combination of these two references as suggested in the Office Action. Cherabuddi discloses partitioning a single cache 23

PAGE 8/11 * RCVD AT 8/25/2004 5:19:36 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):02-52

memory for use by multiple processors 21a, 21b based on the processor mode whereas the Office Action infers the use of separate cache memories 34, 52 from Ingerman is analogous to the claimed memory array. Accordingly, Applicant respectfully submits that again, not only is there no suggestion to combine teachings as set forth in the Office Action in the cited references themselves, the purpose of "flexibility and improved performance" is not an objective reason sufficient to establish *prima facie* obviousness.

Second, it is respectfully submitted that none of the cited references teaches or suggests the claimed limitation of a *memory array adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor while the first portion of the memory array is accessible only by a first processor and the second portion is accessible only by a second processor.* The Office Action alleges this is disclosed by Cherabuddi at par. [0025]. However, while Cherabuddi mentions dynamically allocating resources of cache memory 23 in response to needs of the CPUs, Cherabuddi does not teach or suggest altering the size of the first portion and second portion which still maintain exclusivity for access by respective first and second processors.

Instead, Cherabuddi teaches the opposite by disclosing the ability to alternate partitioning of a single cache memory between two modes as discussed in par. [0009-0011]. That is, a two-thread mode (where both processors are active) and each processor uses a corresponding dedicated portion of the cache memory (i.e., sharing the cache) and a one-thread mode (only one processor is active), where the cache can be entirely allocated such that the active processor can use the entire cache including both memory partitions 23a, 23b. This means that in a one-thread mode, the alleged second memory partition may be accessible by the first processor, in contrast to Applicant's claims.

In response, the Examiner states the Cherabuddi is cited for "dynamically altering a first and second memory portion depending on an operational load of a first and second processor and not for teaching exclusive access to the memory." (5/25/04 Office Action pg. 6). Applicant respectfully submits that the Examiner must consider the teachings of the references in their

PAGE 9/11 * RCVD AT 8/25/2004 5:19:36 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):02-52

entirety, including portions which lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock Inc.*, 721 F.2d 1540 (Fed. Cir. 1983).

It is respectfully submitted that selectively citing passages from prior art references without considering the context in which they are disclosed in an attempt to reconstruct claims in piecemeal fashion based on the hindsight of the Applicant's disclosure is improper and does not establish *prima facie* obviousness. MPEP 2142.

Since Cherabuddi, Uchiyama and/or Ingerman, taken alone or in combination fail to teach or suggest the features of the pending claims, these claims are patentable over the cited art. In view of the foregoing, reconsideration and withdrawal of all §103 rejections are respectfully requested.

CONCLUSION.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below. Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee or deficiency thereof, except for the Issue Fee, is to be charged to **Deposit Account # 50-0221**.

Respectfully submitted,

Stuart A. Whittington
Registration No. 45,215
Intel Corporation
(480) 715-3895

c/o
Blakely, Sokoloff, Taylor & Zafman, LLP

AMENDMENT under 37 C.F.R. § 1.111
U.S. Appln. No. 10/003,170

12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA. 90025-1026
(503) 264-0967

Date: 8/25/04

PAGE 11/11 * RCVD AT 8/25/2004 5:19:36 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:480 715 7738 * DURATION (mm-ss):02-52 P.11